

REMARKS

S1 Regarding Claim 1:

Reference 1 (Patent Application Laid-Open No. Sho 58-192154) cited in the previously issued Notice of the Reasons for Refusal describes a RAM which receives clock pulses (ϕ_1 and ϕ_2) of a predetermined cycle from a CPU; generates the various timing signals therein from its timing generation circuit based on those clock pulses (ϕ_1 and ϕ_2); receives a device ID, an operation code and a RAM address sequentially transmitted by the CPU via a bus; determines by its device comparator whether the received device ID corresponds to its own device ID; and, when that device ID does match its own, transmits data in response to the request concerned.

The various timing signals generated by the timing generation circuit are prepared based on the said clock pulses (ϕ_1 and ϕ_2) (Refer to the upper left column on page 2) and since the data D_1 to D_4 are in synchronism with the clock pulse ϕ_1 according to the time chart in Fig. 4, the RAM in Reference 1 is recognized as a synchronization type RAM which receives a device ID, an operation code and a RAM address and transmits data in response to a request in synchronism with the clock pulses of a predetermined cycle transmitted by the CPU. Because four bits of the data D_1 to D_4 are used for the reception and transmission of such things as a device ID, it is self-evident that there are provided a plurality of output drivers.

S2 Thus, the present invention in Claim 1 and Reference 1 differ in that:

(1) while, in the present invention in Claim 1, the amount of data to be outputted from the memory means is defined according to the read request by an input receiver circuit receiving block size

information specifying the amount of data to be outputted from the memory means in response to the read request in synchronism with an external clock signal, no such arrangement is described in Reference 1, and in that,

(2) while the present invention in Claim 1 is provided with a programmable access time register for storing values indicative of the number of clocks of the external clock signal counted by the time the memory means responds to a read request where it is defined as to after how many clocks the data in response to the read request is to be outputted, no such arrangement is described in Reference 1.

The said differences will now be looked at.

\$3 Difference (1):

It was well known prior to the present application, as from: Patent Appln. Laid-Open No. Sho 60-261095 ("Reference 6") Patent Appln. Laid-Open No. Sho 59-165285 ("Reference 7") to provide a RAM with a function of sequentially and continuously reading data from an address and make it possible to define in the RAM the amount of data to be continuously read by defining from outside and through a bus a value corresponding to the total amount of data to be continuously read, and it is not particularly difficult to designate in the RAM of the invention in Reference 1 from outside via a bus a value corresponding to the total amount of data to be continuously read. Since it is recognizable that the RAM of Reference 1 transmits and receives data in synchronism with clock pulses, a value corresponding to the total amount of data to be continuously read can spontaneously be deduced as received also in synchronism with clock pulses.

\$4 Difference (2):

Reference 4 (Patent Application Laid-Open No. Sho 63-91766) cited in the previously issued Notice of the Reasons for Refusal describes with regard to a data processing system having a central processing unit coupled with an N number of memory means via a bidirectional common bus an invention in which transmission and reception timings corresponding to time periods for having to wait before data read is transmitted on the bus are set with the transmission and reception timing setting circuit provided respectively in the N memory means by a command from the central processing unit whereby efficient access to the memory means is enabled, even if a bidirectional common bus for a narrow data width is used, by transmitting data on the common bus in accordance with the transmission and reception timings the respective memory means are set with in response to a request from the central processing unit for read requests.

Since both References 1 and 4 relate to a system having a central processing unit coupled with memory means via a bidirectional common bus with an aim to improve the efficiency of processing by the system while suppressing any increase to the bus width, it is readily conceivable for a person skilled in the art to apply to the invention of Reference 1 the technical idea of transmitting data on a common bus in response to read requests from the central processing unit in accordance with the transmission and reception timings the respective memory means are set with by commands from the central processing unit.

In Fig. 3 of Reference 4 is an indication of "→ Number of clocks" and lines 13 to 15 of the lower left column on page 2 also read "the number of clocks required for transferring to the central processing unit (CPU) 1 is ..." It can, therefore, be said that timings are grasped in terms of clock numbers in Reference 4 and it is suggested that values expressed in clock numbers are used as the transmission and reception timings the transmission and reception timing setting circuits of the memory means are set with.

Further, it is very common practice to use a register as a means for setting and holding control data like setting and holding a value corresponding to the total amount of data to be continuously read is set and held in References 6 and 7.

§5 Consequently, no special difficulty in creating Difference (2) is recognizable.

Thus, the present invention in Claim 1 was readily conceivable by a person of ordinary skill in the art based on the known techniques described in References 1 and 4 cited in the previous Notice of the Reasons for Refusal.

§6 Regarding Claim 2:

In the invention described in Reference 1, according to Fig. 4, data is outputted in synchronism with the falling edge of the clock pulse, but whether synchronization should be with the rising edge or falling edge is a matter of planning for a person skilled in the art.

§7 Regarding Claim 3:

It is easily conceivable by a person skilled in the art to generate an internal clock signal based on an external clock signal because, even if noise is mixed into the external clock signal line, it does not adversely affect data transmission and reception, and for such various purposes as enhancing the speed of data transfer (Patent Application Laid-Open No. Sho 58-184626 - "Reference 8"); solving the past problems of successive skew between the chips narrowing down the data valid window, thereby violating setup and hold times and causing bus contention (Patent Application Laid-Open No. Hei 2-8950 - "Reference 8"), and for converting a voltage

level when the inner and outer voltage levels are not compatible, like while an external clock signal is of a transistor logic (TTL) level, the interior of the integrated circuit is of a complementary metal oxide semiconductor (CMOS) level (Patent Application Laid-Open No. Sho 63-300310 - "Reference 10"). Data is outputted corresponding to clocks in References 8 and 9 as well.

\$8 Regarding Claim (4):

Refer to Reference 10 and especially to [lines 19-27 on col. 1 of US Patent 4,761,567 corresponding to Reference 10].

\$9 Regarding Claim (5):

In Reference 8, according to Fig. 6, data is outputted in synchronism with the falling edge of the signal V, but whether synchronism ought to be with the rising edge or falling edge is merely a matter of choice for a person skilled in the art.

\$10 Regarding Claim (6):

In Reference 9, a delay locked loop circuit is used.

\$11 Regarding Claim (7):

Since it is common practice in the technical field of computers to set control parameters during the initialization sequence after the terminal is switched on, no special difficulty is recognizable in what is recited in this claim.

\$12 Regarding Claims (8)-(12), (15) and (19):

What are recited in these claims are found described in References 1 and 4. (With regard to Claim 19, refer to Fig. 4.)

S13 Regarding Claims (13) and (14):

It was widely known prior to the present application, as described in Patent Application Laid-Open No. Sho 58-31637 ["Reference 11"], for example, to store a unique identification value to identify the memory device from a plurality of other memory devices.

S14 Regarding Claim (16):

A device ID is programmable in the invention of Reference 1 as well by terminals V1 to V4. In addition, Reference 3 (Patent Application Laid-Open No. Sho 61-107453) cited in the previous Notice of the Reasons for Refusal also discloses an invention making an ID programmable.

S15 Regarding Claim (17):

The invention of Reference 3 is to set an ID by a control circuit. There is no description as to when the setting is achieved but it is obvious that the setting takes place after the module is supplied with power.

S16 Regarding Claim (18):

Whether to employ the method of carrying out precharge immediately after executing a series of read requests to close a page or not to carry out precharge to leave the page open is only

a matter of planning and choice for a person skilled in the art which can be decided in consideration of the merits and demerits of the two (For instance, the former has a demerit of requiring time for the outputting of the first data for its being unable to make use of the page mode in executing the next read request whereas control is easy).

\$17 Regarding Claim (20):

The technical matter recited is the same as that in Reference 6.

\$18 Regarding Claim (21):

Reference 6 discloses a technical idea of defining simultaneously in a single read request a numerical value corresponding to the total amount of data to be read continuously together with the address. Consequently, it can not be considered particularly difficult to include in one request packet in the invention of Reference 1 as well a read request, an address and a total amount of data by making use of any words (fields) being unused among the words X_0 to X_4 or by adding a word X_5 in the instruction format shown in Fig. 3.

\$19 To add, the applicant contends through the Argument that Reference 4 does not disclose or suggest at all the characteristic of the present invention because, according to the technique in Reference 4, the timings set for the respective memory means would not change as long as the corresponding relations between the sequential order of consecutive N number of data and the serial numbers of N memory means remain the same but such timings do change when the corresponding relations between the order of those N data and serial numbers of those N memory means vary and, after all, the

timings have to be set every time a read request is issued or before each read request is issued.

As to whether or not it is necessary to set timings every time a read request is issued is not a contention relevant to the recitation of claim. Moreover, in Reference 4, it is readily perceivable by a person skilled in the art that it suffices to set timings for the memory means only in case the corresponding relations between the order of N consecutive data and the serial numbers of N memory means vary, and it can only be said that the applicant's assertion that "after all, the timings have to be set every time a read request is issued or before each read request is issued" is inappropriate.

Thence, the applicant's said contention is not acceptable.

§20 Thus, the inventions recited in Claims 1 to 21 were readily conceivable by anyone skilled in the art and can not be patented pursuant to Article 29, paragraph 2 of the Patent Law.

§21 Further, the applicant need be made aware of also the following:

(1) The recitations of Claims 7, 8 and 17 are to define when a value is to be set for the register and not to define the construction of an article. It is indeterminate, therefore, whether the inventions in those claims are in the category of articles or methods (This is in contradiction of Article 36, paragraph 5, item 2 and paragraph 6 of the Patent Law).

§22 (2) It is unclear which description in the specification the recitation "[output drivers (76)] output data synchronously with respect to a rising edge transition of the external clock signal (53, 54)" as amended is based on. It appears that the expression "synchronously with respect to a rising edge" specifies outputting

of data at the timing of a rising edge (as a trigger). But, as clear from the descriptions in [the original English text, page 56, line 21 to page 57, line 2] reading "One important part of the input/output circuitry generates an internal device clock based on early and late bus clocks. Controlling clock skew (the difference in clock timing between devices) is important in a system running with 2 ns cycles, thus the internal device clock is generated so the input sample and the output driver operate as close in time as possible to midway between the two bus clocks" and in [the original English text, page 58, lines 23 and 24] reading that "The gate delay between the internal device clock and output circuits driving the bus", the output drivers in the present invention are operated to output data in synchronism with the rising edge (or falling edge) of the internal device clock generated by early and late bus clocks. Because the internal device clock is of nearly an intermediate phase between the early bus clock and the late bus clock, the rising edge of the internal device clock and the rising edges of early and late bus clocks are mutually shifted in timing and not the same. The basis for the amendment in Claim 2 to read "output data synchronously with respect to a rising edge transition of the external clock signal (53, 54)" is, therefore, unclear.